LISTING OF CLAIMS

1. (Original) A digital-to-analog converter to convert into an analog quantity a digital code including a first part of more significant bits and a second part of less significant bits, comprising:

a first section to convert the first part of the digital code into a first voltage, said first voltage being of discrete voltages that are integral multiples of a predetermined first voltage step;

a second section to convert the second part of the digital code into a current;

means for transforming the current of the second section into a second voltage, said second voltage being of discrete voltages that are integral multiples of a second voltage step equal to 1/2L of the product of the first voltage step multiplied by a predetermined coefficient, where L is the number of the less significant bits of the digital code to be converted;

control means of the first and the second section; and

summation means for generating the analog quantity as the sum of the second voltage and the product of the first voltage multiplied by the predetermined coefficient, comprising a summation circuit with resistive feedback means including a voltage divider; and

wherein the means for transforming the current into a second voltage comprises a conversion resistor that forms part of the voltage divider.

2. (Original) The converter in accordance with Claim 1, wherein

the summation circuit comprises an operational amplifier having a first input, a second input and an output connected to the converter output;

the predetermined coefficient is the gain of the operational amplifier;

the voltage divider of the resistive feedback means is connected between the output and the first input of the operational amplifier;

the first section comprises a resistive network having 2M taps, where M is the number of the more significant bits of the digital code to be converted, and substantially equal resistances between adjacent taps, and 2M electronic switches each inserted between a respective tap and a common node connected to the second input of the operational amplifier;

the second section comprises a group of L current generators presented in binary form, selection means of the L current generators and means for conveying the current of the selected generators onto a common node connected to the conversion resistor; and

the control means comprise means for selectively operating the electronic switches in such a way as to individually connect each of the 2M taps to the second input of the operational amplifier according to the first part of the digital code and means for selectively operating the selection means of the current generators according to the second part of the digital code.

3. (Original) The converter in accordance with Claim 2, wherein the second section comprises a further group of L current generators presented in binary form and further selection means of the L further current generators and wherein the control means comprise a selection logic that alternatively activates the use of either one or the other group of generators according to whether the digital code to be converted does or does not exceed, respectively, a predetermined value.

4. (Original) The converter in accordance with Claim 1, wherein

the summation circuit comprises an operational amplifier having a first input, a second input and an output connected to the output of the converter;

the predetermined coefficient is the gain of the operational amplifier;

the voltage divider of the resistive feedback means is connected between the output and the first input of the operational amplifier;

the first section comprises a resistive network having 2M-1 taps, where M is the number of the more significant bits of the digital code to be converted, and substantially equal resistances between adjacent taps, and 2M-1 electronic switches, each inserted between a respective tap and a common node connected to the second input of the operational amplifier;

the second section comprises a group of L current generators presented in binary form, selection means of the L current generators, a further group of current generators, of which L are presented in binary form and one complementary generator having the same weight as the generator of smallest weight of the L current generators, further selection means of the further group of current generators and means for conveying onto a common node, connected to the conversion resistor, the current of the selected generators;

the control means comprise means for selectively operating the electronic switches in such a way as to individually connect each of the 2M-1 taps to the second input of the operational amplifier according to the first part of the digital code, means for selectively operating the selection means of the current generators according to the second part of the digital code and a selection logic that alternatively activates the use of one or the other group of

generators according to whether the digital code to be converted does or does not exceed, respectively, a predetermined value.

5. (Original) The digital-to-analog converter in accordance with Claim 4, wherein the electronic switches of the first section form a first and a second group of electronic switches having an electronic switch in common and wherein the selection logic determines the operation of the electronic switches of the first or the second group according to whether the digital code to be converted does or does not exceed, respectively, a predetermined value and determines the permanent selection of the complementary generator of the further group of current generators when the digital code to be converted does not exceed the predetermined value.

6. (Original) A converter in accordance with Claim 5, wherein the further current generators of the second group comprise P-channel MOS transistors.

7. (Original) The converter in accordance with Claim 4, wherein the predetermined value is expressed by the digital code having the most significant bit equal to 0 and the remaining bits equal to 1.

8. (Original) The converter in accordance with Claim 4, wherein the current generators of the second group comprise N-channel MOS transistors.

9. (Original) A converter in accordance with Claim 3, wherein the further current generators of the second group comprise P-channel MOS transistors.

Claims 10-21. (Canceled).

22. (Currently Amended) A circuit, comprising:

a more significant bit converter having an analog voltage output indicative of a more significant bit portion of an input digital signal;

a less significant bit converter having an analog current output indicative of less significant bit portion of the input digital signal;

a summation circuit including a first input terminal coupled to the analog voltage output and a second input terminal; and

a feedback path coupled between the second input terminal and an output of the summation circuit and connected to the analog current output;

wherein the less significant bit converter comprises:

a first plurality of current generators;

a second plurality of current generators; and

a selection circuit that selectively connects one or more of the first and second plurality of current generators to the analog current output ~~, or alternatively selectively connects one or more of the second plurality of current generators to the analog current output,~~ based ~~at least in part~~ on a combination of the less significant bit portion and the more significant bit portion of the input digital signal.

23. (Currently Amended) The circuit of claim 22 wherein the selection circuit alternatively chooses between connection of the first and second plurality of current generators based on the more significant bit portion of the input digital signal and chooses certain ones of the generators for connection based on the less significant bit portion of the input digital signal.

24. (Original) The circuit of claim 22 further comprising a current mirror circuit that mirrors, for use by the first and second plurality of current generators, a current which is flowing in the more significant bit converter.

25. (Currently Amended) A circuit, comprising:

a more significant bit converter having an analog voltage output indicative of a more significant bit portion of an input digital signal;

a less significant bit converter having an analog current output indicative of less significant bit portion of the input digital signal;

a summation circuit including a first input terminal coupled to the analog voltage output and a second input terminal; and

a feedback path coupled between the second input terminal and an output of the summation circuit and connected to the analog current output;

wherein the less significant bit converter comprises:

a first plurality of current generators;

a second plurality of current generators; and

a selection circuit that selectively connects one or more of the first plurality of current generators to the analog current output, or alternatively selectively connects one or more of the second plurality of current generators to the analog current output, based at least in part on the less significant bit portion of the input digital signal ~~The circuit of claim 22~~,

wherein the feedback path comprises a first and second resistor connected to each other at a node to form a series voltage divider, the node in the feedback path being connected to the analog current output.

26. (New) The circuit of claim 25 wherein the selection circuit chooses between connection of the first and second plurality of current generators based on the more significant bit portion of the input digital signal.

27. (New) The circuit of claim 25 further comprising a current mirror circuit that mirrors, for use by the first and second plurality of current generators, a current which is flowing in the more significant bit converter.

28. (New) A circuit, comprising:

a more significant bit converter having an analog voltage output indicative of a more significant bit portion of an input digital signal;

a less significant bit converter having an analog current output indicative of less significant bit portion of the input digital signal;

a summation circuit including a first input terminal coupled to the analog voltage output and a second input terminal; and

a feedback path coupled between the second input terminal and an output of the summation circuit and connected to the analog current output;

wherein the less significant bit converter comprises:

a first plurality of current generators;

a first selection circuit operable to selectively connect one or more of the first plurality of current generators to source current to the analog current output based at least in part on the less significant bit portion of the input digital signal;

a second plurality of current generators; and

a second selection circuit operable to selectively connect one or more of the second plurality of current generators to sink current from the analog current output based at least in part on the less significant bit portion of the input digital signal.

29. (New) The circuit of claim 28 wherein the first and second selection circuits choose to make selective connection of the first and second plurality of current generators based additionally on the more significant bit portion of the input digital signal.

30. (New) The circuit of claim 28 further comprising a current mirror circuit that mirrors, for use by the first and second plurality of current generators, a current which is flowing in the more significant bit converter.

31. (New) The circuit of claim 28, wherein the feedback path comprises a first and second resistor connected to each other at a node to form a series voltage divider, the node in the feedback path being connected to the analog current output.